Optical Data Transmission from the CMS Cathode Strip Chamber Peripheral Trigger Electronics to Sector Processor Crate

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Abstract

The Muon System of the Compact Muon Solenoid (CMS) experiment at CERN consists of three detectors: Cathode Strip Chambers (CSC), Drift Tubes (DT) and Resistive Plate Chambers (RPC). The CSC front end electronics is located on chambers as well as in the 9U VME crates. The Trigger Motherboard (TMB) matches anode and cathode tags called Local Charged Tracks (LCT) and sends the two best combined LCTs from each chamber to the Muon Port Card (MPC). Each MPC collects data representing muon tags from up to nine TMB, which corresponds to one sector of CSC chambers.

All TMB and MPC cards are located in 9U*400 mm VME crates mounted on the periphery of return yoke of the endcap muon system. Several TMB modules communicate with one MPC residing in the same crate over a custom peripheral backplane. The MPC selects data representing the three best muons and sends it over optical links to the Sector Receiver (SR) residing in the counting room 100 meters from the detector. The current electronics layout assumes 48 MPC modules residing in the 48 peripheral crates for both muon endcaps and 24 SR residing in the counting room. Each SR reformats the track segments into global coordinates suitable for the track-finding algorithms at the Sector Processor Board [1]. At the present design one SP board communicates with three SR over custom backplane.

Due to high operating frequency of 40.08MHz and the long distance from the detector to counting room an optical link is the only choice for data transmission. Our goal was to prototype a communication link between the MPC and SR using existing commercial components and evaluate possible options for the final link implementation.

I. CHOICE OF CHIPSET FOR DATA SERIALIZATION AND OPTICAL MODULE

An overview of the requirements for the front end serializer/deserilizer chipsets in LHC environment can be found in [2]. Two Agilent (former Hewlett-Packard) chipsets (5V HDMP-1022/1024 and 3.3V HDMP-1032/1034) have some advantages over other commercial components. Among them for the HDMP-1022/1024: flexible choice of operating range (150-1500 Mbaud, user selectable), flexible and wide enough parallel interface (16, 17, 20 or 21 bits), and choice of synchronization to either fill frames or a receiver reference oscillator. Unfortunately, both chipsets are not pin compatible and 20- or 21-bit interface is available for the 1022/1024 chipset only. A lot of experience with the 1022/1024 chipset was gained by several research groups working in particle physics [3]. At the time of our design the final specification of 1032/1034 chipset was not available, so we chose the 1022/1024 chipset for our prototyping.

Optical transmitter and receiver modules are available from several manufacturers, including Infineon, Molex, Finisar, Methode and some others. We chose a Methode MDX-19-4-1-T multimode (850 nm) optical transceiver. The required data rate (20 bit @ 40 MHz) is within the specified range for this module (1.25 Gbaud maximum). This optical module is available in industry standard 1x9 package with SC fiber optic connector. It was also evaluated by other groups and reliable operation was demonstrated.

II. DESIGN IMPLEMENTATION

Simplex data transmission from the MPC to SR was used. Instead of adding a return path for link control and monitoring we perform all necessary procedures for link initialization, reset and resynchronization over VME which is the main control path for the peripheral electronics residing in the 9U crates.

The main part of the Muon Port Card is a sorter unit which selects data representing three best muons out of 18 possible. This data word contains 120 bits listed in Table 1.

Table 1: Trigger Data from MPC to SR

Signal	Bits per 1 muon	Bits per 3 muons
Valid Pattern Flag	1	3
Cathode Pattern Number (0-255)	8	24
Cathode Left/Right Bend (0/1)	1	3
Cathode ½-Strip ID (0-159)	8	24
Anode Pattern Quality (0-3)	2	6
Accelerator Muon	1	3
Anode Wire Gang ID (0-111)	7	21
CSC ID (0-8)	4	12
Anode Bunch Crossing (0-31)	5 (*)	5
Data Error	1 (*)	1
Status Bits	6	18
Total	44	120

* Common bits to 3 muons

120 bits of data are sent out of the sorter unit into serializer inputs every 25 ns of the LHC main frequency of 40.08MHz. Six HDMP-1022 transmitters convert data into serial streams and send them to six Methode MDX-19-4-1-T optical transceivers. At the receiver end six matching optical modules provide serial streams to HDMP-1024 deserializer chips which convert them into parallel form. The existing SR prototype receives data from two MPC, or 240 bits of data total every 25 ns, so twelve optical modules and twelve HDMP-1024 receivers are needed in order to serve two MPCs. Several front end FPGA chips at the SR provide an alignment of incoming from two MPC data for the further conversion in LUT RAMs. After that the data in suitable format is transmitted over a custom backplane to Sector Processor module residing in the same crate for further processing.

We have implemented a simplex scheme 3 without return path as described in datasheet [4]. The transmitter uses the main 40.08MHz frequency as the reference and data clock. At the receiver end, an external reference oscillator with slightly different frequency of 40.04MHz is used for frequency acquisition during synchronization. The 21st bit was enabled as an alternating "Flag" for enhanced framing "Error" detector in order to improve the synchronization process. Our configuration can also force periodic transmission of "Fill Frames" to additionally verify and achieve proper framing in the presence of repetitive data. We have used the layout tips proposed in [5] for the HDMP-1022/1024 chipset layout and found them very helpful. Optical cables are directed to the front panel of MPC and rear end of SR.

III. PROTOTYPING RESULTS AND FUTURE DESIGN IMPROVEMENTS

Prototypes of the MPC and SR were built and tested in summer of 2000. Two modules were connected via 100 m optical cables and test patterns were sent from MPC output FIFO buffer, received into SR input FIFO and checked against each other. Our designs have demonstrated a reliable operation at 40MHz.

High power consumption (1.9W per one HDMP-1022 and 2.5W per one HDMP-1024) and the large board space required for optical modules and the serializers or deserializers are drawbacks of our implementation. One of the future improvements would be to utilize the latest Agilent HDMP-1032/1034 chipset for serialization and deserialization. Power consumption can be reduced up to 0.56W for the

HDMP-1032 transmitter and 1.0W for the HDMP-1034 receiver. Unfortunately, the 20-bit mode is not available for this chipset and 8 HDMP-1032/1034 chipsets instead of six HDMP-1022/1024 would allow us to transmit the same amount of bits. Double-frame mode (two 16-bit frames sent in one clock cycle) is supported by HDMP-1032/1034 chipset, but at 40MHz the overall data rate would be 1.6Gbaud which is outside the specified range for this chipset (1.4Gbaud maximum).

Another option would be to use the commercial serializers and deserializers running at higher frequencies (typically 80..125MHz) which are available from several vendors (Motorola, TI, Vitesse, PMC-Sierra). Particularly we are interested in the TI family of multigigabit transceivers TLK2500/2501.

Small form factor single-channel optical modules can be used for a more compact design. Another approach is to use multi-channel optical receivers and transmitters. Such 8- or 12-channel devices are available from Infineon [6] and Optobahn [7]. They can save a lot of board space, but also require an external serializers and deserializers for parallel-to-serial and serial-to-parallel data conversion.

We also can use an appropriate commercial or custom solution adopted by other CMS groups. One custom 1.25Gbit/s transmitter ASIC is currently under design at CERN-EP/MIC [8]. It is particularly desirable for our application because of the resistance to high radiation doses and operational tolerance to a single event upsets. Another design of a custom radiation tolerant serializer was proposed for ATLAS experiment [9].

IV. Conclusion

We have built and tested prototypes of the Muon Port Card and Sector Receiver modules which provide optical trigger data transmission from the peripheral CSC crates to the counting room. Data transmission circuitry is based on commercial components and has demonstrated reliable operation at 40MHz. Future improvements to this optical path can be based on small form factor optical transceivers or multi-channel modules. Use of either low power commercial serializers and deserializers or custom circuits will allow us to enhance the electrical interface of the data transmission circuitry.

V. References

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